ABSTRACT

An improved and new process, used for the elimination of copper line damage, copper defects, non-uniformity improvement, with low dishing and erosion, in damacene processing, is disclosed. This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically to the elimination of copper line damage for damascene processing, by depositing a multilayer interface material, consisting of a mechanically hard film and a soft film, over a low dielectric constant, interlevel metal dielectric (IMD), and subsequently chemical mechanical polishing (CMP) back the excess material to planarize the surface.